

Amendments to the Claims:

The listing of claims will replace all prior versions and listing of claims in the application:

Listing of claims:

1. (Cancelled)

2. (Previously Presented) In an integrated circuit (IC) having faults to be tested by fault simulation using a test of a plurality of tests, each test including an input test vector, a method for improving the efficiency of the fault simulation comprising:
 - a) performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC;
 - b) based on the good machine simulation, identifying potential faults to be tested by the test by backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node, said backtracing being based on outputs of said logic gates and memory elements, the outputs being obtained from said good machine simulation said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node;
 - c) with the test, performing the fault simulation on the potential faults to be tested; and
 - d) repeating a) through c) for additional tests of the plurality of tests.

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Previously Presented) The method as recited in claim 2, wherein observed results of the test further limit a number of faults requiring processing by the fault simulation by starting the backtraces from only observable nodes wherein the faults to be tested were detected.

7. (Cancelled)

8. (Previously Presented) In an integrated circuit (IC) having a fault to be tested by fault simulation using a test of a plurality of tests, each test of the plurality of tests including an input test vector, a method for improving the efficiency of the fault simulation comprising:

a) performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC;

b) based on the good machine simulation, identifying potential faults in the IC that are blocked by the test from being observed at an observable point of said IC by backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node, said backtracing being based on outputs of said logic gates and memory elements, the outputs being obtained from said good machine simulation said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node;

c) with the test, performing the fault simulation on the potential faults that were identified as not being blocked; and

d) repeating a) through c) for each test of the plurality of tests.

9. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method for improving the efficiency of a fault simulation of an integrated circuit (IC) having a fault to be tested by the fault simulation using test, each of said tests including an input test vector, said method comprising:

- a) performing a good machine simulation on the IC with the test to obtain values of each internal node of the IC;
- b) based on the good machine simulation, identifying potential faults in the IC that are blocked by the test from being observed at an observable point of said IC by backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node, said backtracing being based on outputs of said logic gates and memory elements, the outputs being obtained from said good machine simulation said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node;
- c) with the test, performing a fault simulation on the potential faults that were identified as not being blocked; and
- d) repeating a) through c) for each test of the plurality of tests.

10. (Previously Presented) A computer program product comprising: a computer usable medium having computer readable program code means embodied therein for improving the efficiency of a fault simulation of an integrated circuit (IC) having a fault to be tested by the fault simulation using a test of a plurality of tests, each test of the plurality of tests including an

input test vector, the computer readable program code means in said computer program product comprising:

- a) computer readable program code means for causing a computer to perform good machine simulation on the IC with the test to obtain values of each internal node of the IC;
- b) computer readable program code means for causing the computer to identify potential faults in the IC that are blocked by the test from being observed at an observable point of the IC, based on the good machine simulation by backtracing, in a single detection pass, through logic gates and memory elements of the IC, starting at each observable node, said backtracing being based on outputs of said logic gates and memory elements, the outputs being obtained from said good machine simulation, said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node;
- c) computer readable program code means for causing the computer to perform the fault simulation on the potential faults that were identified as not being blocked with the test; and
- d) computer readable program code means for causing the computer to repeat a) through c) for each test of the plurality of tests.

11. (Previously Presented) The method as recited in claim 8, wherein observed results of the test further limit a number of faults requiring processing by the fault simulation by starting the backtraces from only observable nodes wherein the fault was detected.

12. (Previously Presented) The device as recited in claim 9, wherein observed results of the test further limit a number of faults requiring processing by the fault simulation by starting the backtraces from only observable nodes wherein the fault was detected.

13. (Previously Presented) The product as recited in claim 10, wherein observed results of the test further limit a number of faults requiring processing by the fault simulation by starting the backtraces from only observable nodes wherein the fault was detected.